

Notice of References Cited	Application/Control No. 10/674,682	Applicant(s)/Patent Under Reexamination ELBOIM ET AL.	
	Examiner JESSE DILLER	Art Unit 2187	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Prototype validation is key to working silicon", Edited by the Electronicstalk editorial team Mar 22, 2001, downloaded from http://www.electronicstalk.com/news/ims/ims100.html on 12/16/2008.
	V	Robert Madge, Brady R. Benware, W. Robert Daasch, "Obtaining High Defect Coverage for Frequency-Dependent Defects in Complex ASICs". IEEE Design & Test of Computers, Sept. 2003. pages 46-53.
	W	Kee Sup Kim, Subhasish Mitra, and Paul G. Ryan, "Delay Defect Characteristics and Testing Strategies". IEEE Design & Test of Computers, Sept. 2003. pages 8-16.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.